

What is claimed is:

1 1. A test device for detecting alignment of active
2 areas and memory cell structures in DRAM devices with vertical
3 transistors, wherein the test device is disposed in a scribe
4 line region of a wafer, comprising:

5 parallel first and second memory cell structures
6 disposed in the scribe line region, each having a
7 deep trench capacitor and a transistor structure;
8 an active area disposed between the first and second
9 memory cell structures, wherein the active area
10 overlaps the first and second memory cell
11 structures a predetermined width; and

12 first to fourth conductive pads disposed on both ends
13 of the first and second memory cell structures
14 respectively.

1 2. The test device as claimed in claim 1, wherein a
2 first resistance is measured by the first and second
3 conductive pads disposed on both ends of the first memory cell
4 structure, and a second resistance is measured by the third
5 and fourth conductive pads disposed on both ends of the second
6 memory cell structure, and alignment shift (ΔW) of the active
7 area and the first and second memory cell structures is
8 estimated according to the first resistance, the second
9 resistance, and the predetermined width.

1 3. The test device as claimed in claim 2, wherein the
2 alignment shift (ΔW) is estimated according to an equation

3 of $\Delta W = W \times \frac{(R2 - R1)}{(R2 + R1)}$;

4 wherein R1 is the first resistance, R2 is the second
5 resistance and W is the predetermined overlap width between
6 the active area and the first and second memory cell structures
7 respectively.

1 4. The test device as claimed in claim 1, wherein the
2 first to fourth conductive pads are made of polysilicon.

1 5. The test device as claimed in claim 1, wherein the
2 wafer further has a memory region including a plurality of
3 memory cells with vertical transistors.

1 6. A method for detecting alignment of deep trench
2 capacitors and word lines in DRAM devices with vertical
3 transistors, comprising:

4 providing a wafer with at least one scribe line region
5 and at least one memory region;

6 forming a plurality of memory cells with vertical
7 transistors in the memory region and at least one
8 test device in the scribe line simultaneously with
9 the same masks and process, the test device
10 including:

11 parallel first and second memory cell structures
12 disposed in the scribe line region, each
13 having a deep trench capacitor and a
14 transistor structure;

15 an active area disposed between the first and second
16 memory cell structures, wherein the active
17 area overlaps the first and second memory cell
18 structures a predetermined width; and

19 first to fourth conductive pads disposed on both
20 ends of the first and second memory cell
21 structures respectively;
22 detecting a first resistance between the first and second
23 conductive pads disposed on both ends of the first
24 memory cell structure, and a second resistance
25 between the third and fourth conductive pads
26 disposed on both ends of the second memory cell
27 structure;
28 determining alignment of the active area and the first
29 and the second memory cell structure according to
30 the first resistance and the second resistance; and
31 determining alignment of the active area and the memory
32 cells in the memory regions according to alignment
33 of the active area and the first and the second
34 memory cell structures of the test device.

1 7. The method as claimed in Claim 6, further comprising
2 a step of determining alignment shift (Δw) of the active area
3 and the first and the second memory cell structures according
4 to the first resistance, the second resistance, and the
5 predetermined width between first and second memory cell
6 structures and the active area respectively.

1 8. The method as claimed in Claim 7, wherein the
2 alignment shift (ΔW) is estimated by an equation:

3
$$\Delta W = W \times \frac{(R2 - R1)}{(R2 + R1)};$$

4 wherein W is the predetermined overlap width between
5 first and second memory cell structures and the
6 active area respectively; R1 is the first

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7 resistance between the first and second conductive
8 pads disposed on both ends of the first memory cell
9 structure; and R2 is the second resistance between
10 the third and fourth conductive pads disposed on
11 the second memory cell structure.